

ABSTRACT

A method and apparatus for monitoring the response times of computer system components in order to improve computer system reliability and performance are provided. The method and apparatus are particularly applicable to computer systems with memory circuits, such as SLD RAMs, that have programmable response times. A response time monitoring circuit in the form of a phase detector includes a plurality of flip-flops with the data inputs commonly connected to receive a response ready signal from a component, such as a memory circuit, in response to a command to perform a task. Each clock input of the flip-flop is connected to a clock signal at a different phase of a response period. The outputs of the flip-flops determine the phase at which the response ready signal was generated by the component.